Confirmation No.8293

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	EL-FARHANE	Examiner:	Chhaya, S.
Serial No.:	10/554,067	Group Art Unit:	2822
Filed:	October 21, 2005	Docket No.:	FR030044US1
Title:	SEMICONDUCTOR DEVICE COMPRISING EXTENSIONS PRODUCED FROM MATERIAL WITH A LOW MELTING POINT		

APPEAL BRIEF

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P.O. Box 1450
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65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed October 6, 2008 and in response to the rejections of claims 1-11 as set forth in the Final Office Action dated April 17, 2008.

Please charge Deposit Account number 50-0996 (NXPS.390PA) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 018118/0468 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-11 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated June 4, 2008.

V. Summary of Claimed Subject Matter

The following summary is made in connection with the independent claims and exemplary reference to example embodiments to which the claims may apply.

In accordance with independent claim 1, an example embodiment is directed to a semiconductor device having a gate electrode, a gate insulating layer, a source region and a drain region (*see*, *e.g.*, 1, 2, 4 and 5 respectively, as described at paragraphs 0016-0017). The gate electrode and the gate insulating layer are produced on a part of the surface of a substrate of a first semiconductor material having a given melting point (*e.g.*, 10 of FIG. 1), and surrounded by an insulating spacer (*e.g.*, 3 of FIG. 1) in a plane parallel to the surface of the substrate. The gate insulating layer is disposed between the substrate and the gate electrode. The source region and the drain region are situated under the surface of the substrate at the level of two opposite sides of the gate electrode, respectively. Each source and drain region includes electrical carriers of the same given type, with respective first concentrations (*see*, *e.g.*, paragraph 0016), and a portion of a

second semiconductor material disposed on the substrate below the level of the gate insulating layer in a direction perpendicular to the surface of the substrate(*see*, *e.g.*, 6 and 7 of FIG. 1 and paragraphs 0018-0019). Each portion of second material extends at least partially between the substrate and the spacer, substantially as far as a limit coming in line, in said perpendicular direction, with one side of the gate electrode. The portions of the second material are doped with doping elements in order to create electrical carriers of said given type with second concentrations less than said first concentrations, and said portions of the second material have a melting point lower than the melting point of the first material.

In accordance with independent claim 7, another example embodiment is directed to a method of manufacturing a semiconductor device, the method including the following steps, with exemplary reference made to Figures 2-7 and paragraphs 0021-0027. A gate insulating layer (2) is formed on a part of a surface of a substrate of a first semiconductor material (100) having a given melting point, and a gate electrode (1) is formed on top of the gate insulating layer. An insulating spacer (3) is formed, disposed around the gate insulating layer and the gate electrode, parallel to the surface of the substrate. Two surface films of the first material are removed respectively in two lateral parts of the surface of the substrate situated on two opposite sides of the surface part of the substrate carrying the gate insulating layer and the gate electrode (P2, P2 in FIG. 3). Each lateral part extends between the substrate and the spacer substantially as far as a limit coming in line with one of the opposite sides of the gate electrode, in a direction perpendicular to the surface of the substrate. A source region and a drain region (4 and 5) are formed, each region being situated below the surface of the substrate at a level of said two lateral parts of the surface of the substrate, respectively, each region containing electrical carriers of the same given type with respective first concentrations. A portion of a second semiconductor material is formed on the substrate, in each lateral part, substantially as far as a limit coming in line, in said perpendicular direction, with the opposite side of the gate electrode corresponding to said lateral part (6 and 7). The portions of the second material contain doping elements in order to create electrical carriers of the given type, and have a melting point lower than the melting point of the first material (*see*, *e.g.*, paragraph 0025). The portions of second material are heated to a temperature intermediate between the respective melting points of the first and second

materials, so that the portions of second material contain electrical carriers with second concentrations lower than said first concentrations (*see, e.g.*, paragraph 0027).

VI. Grounds of Rejection to be Reviewed Upon Appeal

1. Claims 1-3 and 6 stand rejected under 35 U.S.C. § 102(b) over Wieczorek *et al.* (US Patent No. 6,274,894).

2. Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) over Wieczorek *et al.* (US Patent No. 6,274,894) in view of Chau *et al.* (US Patent No. 5,710,450).

3. Claims 7-11 stand rejected under 35 U.S.C. § 103(a) over Chau *et al.* (US Patent No. 5,710,450) in view of Andideh *et al.* (US Patent No. 6,121,100) and further in view of Wieczorek *et al.* (US Patent No. 6,274,894).

VII. Argument

Appellant notes that no response was made to the Appellant's Final Office Action Response, in the form of an Advisory Action or otherwise. In this regard, the following argument incorporates various aspects of the Final Office Action Response, with emphasis on errors in all rejections. In short, the rejections rely upon unsupported allegations of inherent structures that fail to meet the requirements for establishing inherency (relative to structure *necessarily* present), and the cited reference(s) do not provide correspondence to multiple claim limitations. The following more particularly addresses these matters.

1. The Section 102(b) rejection of claims 1-3 and 6 over the '894 reference must be reversed because the rejection relies upon unsupported allegations of "inherent" limitations, and further because the '894 reference does not disclose the claim limitations as asserted.

A. The Office Action's allegations of inherency are erroneous.

The Office Action's allegations of inherency are in violation of both the M.P.E.P. and relevant law, and the rejection thus fails to establish correspondence to the claimed invention. These allegations have failed to cite to any reference that discloses the allegedly "inherent" structure, rely upon a "claim 3" without identifying whether the claim is from the cited reference or the instant application, and further rely upon an

erroneous interpretation of semiconductor materials and their relative properties. To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269 (quoting *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981).

Referring to independent claim 1, the Office Action has attempted to show correspondence to the claimed second source/drain material and its relative melting point by asserting that the lightly-doped drain (LDD) 56 of the '894 reference inherently has "a melting point lower than the melting point of the" source/drain 60 based upon "the materials claimed in claim 3." Claim 3 of the '894 reference recites a carrier type of such a LDD type region, but fails to mention anything about a melting point. Various other portions of the '894 reference mention different materials for the LDD 56 (*e.g.*, as recited in the rejection of claim 3), but do not disclose using respective materials as the LDD 56 and drain 60 such that the LDD 56 has a lower melting point. In this context, the Office Action has provided no support for the allegedly inherent LDD 56 and source/drain 60 materials and their respective melting point characteristics, and has not demonstrated that such characteristics are necessarily present in the '894 reference.

Should the Office Action be referring to "claim 3" of the instant application, this attempt to assert that the '894 reference's disclosure of similar materials for the LDD 56 "inherently" corresponds to the claimed invention is clearly erroneous. While the '894 reference discloses that the LDD 56 may be "formed from a silicon-germanium alloy" where the source/drain 60 is silicon-based (similar to claim 3), this assertion stops far short of disclosing that the LDD 56 must *necessarily* have a melting point that is lower than the melting point of the source/drain 60. Nothing in the Office Action, the instant application or the cited references demonstrates that such a relationship *necessarily* exists, simply because respective silicon-germanium and silicon materials are used. For instance, there are a multitude of different alloys based on silicon-germanium, and a corresponding multitude of different materials including silicon-based materials. In addition, the respective LDD 56 and source/drain regions 60 may also be doped (*e.g.*, as

in claim 3 of the '894 reference), which would clearly affect a variety of properties. The Office Action's assertions are akin to suggesting that any and all materials "based on germanium or based on an alloy of silicon and germanium" must have a melting point that is lower than the melting point of any and all materials "based on silicon." Clearly, this assertion is erroneous as various types of such materials may exist. Moreover, a single common material that is "based on silicon" may be an alloy of silicon and germanium, such that the indicated materials would be the same (and have the same melting point). In this regard, the allegedly "inherent" structures with respective melting points are not "necessarily" present in the '894 reference, in view of claim 3 of the instant application or otherwise.

In this regard, the Section 102(b) rejections are improper because the allegedly inherent functions are in violation of the M.P.E.P. and relevant law. Appellant further submits that the rejections are improper because they have failed to identify which subject matter in the asserted "claim 3" is relied upon, such that the rejections are unclear and fail to meet the requirements of Section 102(b) or 35 U.S.C. §132.

B. The '894 reference fails to disclose multiple claim limitations.

As consistent with Appellant's Responses of record, the '894 reference does not disclose limitations directed to "each portion of second material extending at least partially between the substrate and the spacer, substantially as far as a limit coming in line, in said perpendicular direction, with one side of the gate electrode." The cited LDD 56 in the '894 reference is clearly aligned to the dielectric 50 adjacent the sidewall of the gate 44 and fails to extend to a line perpendicular to the sidewall of the gate 44 itself (*see, e.g.*, figures 7-9 in the '894 reference). This contradicts the claimed structure, as exemplified in FIG. 7 of the instant application, showing example second material 6 and 7 aligned to the gate 1 and further directly below spacers 30.

For convenience, Appellant has copied FIG. 9 of the '894 reference and FIG. 7 of the instant application below.

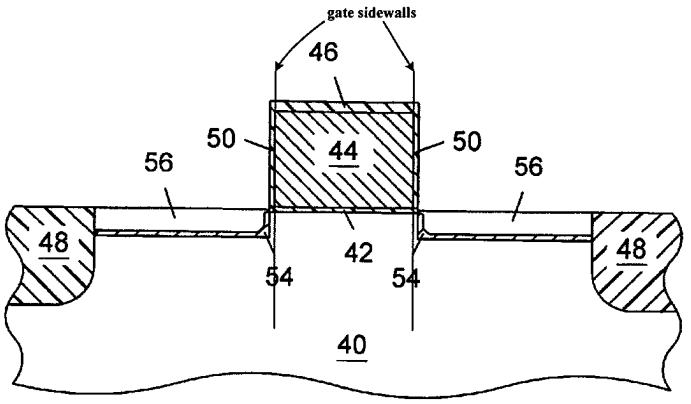

Fig. 9

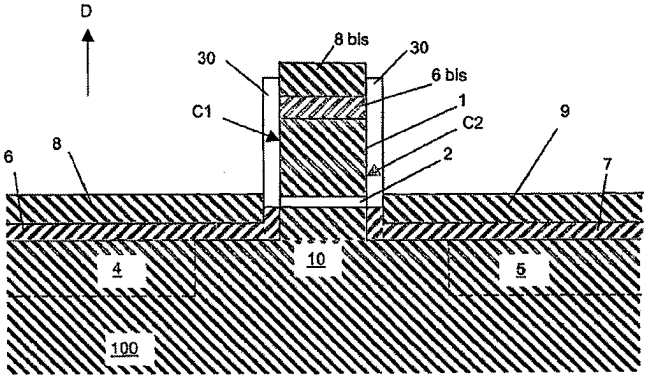

FIG. 7

FIG. 9 of the '894 reference clearly shows that the LDD 56 is formed in a trench that is self-aligned to the *outside* edges of the dielectric sidewalls 50, thus offsetting the LDD 56 from the gate 44 and further restricting the LDD 56 from formation below the sidewalls 50. In contrast, FIG. 7 of the instant application shows 6 and 7 disposed below the sidewall spacers 30 and directly in line with the sides C1 and C2 of the gate 1. It appears that the Examiner is confusing the silicon portions 8 and 9 of FIG. 7 with the claimed second material (as may correspond to 6 and 7), based upon the response to arguments section of the Final Office Action, and thus has failed to overcome Appellant's arguments regarding claimed second material. In this context, Appellant submits that the Section 102 (b) rejections are improper and must be reversed.

In view of the above, the Office Action has failed to establish correspondence between the '894 reference and claim limitations directed to materials of respective melting points. As all claims are directed to subject matter relating to these melting points and as all rejections rely upon these misapplied citations to the '894 reference, all rejections must be reversed. In short, the cited references, alone or in combination, fail to disclose aspects of the invention directed to semiconductor materials of differing melting points, the corresponding structure, and the method of manufacture such a structure as related to the use of materials with relative melting points as claimed. The cited references simply do not comprehend or disclose the claimed invention. The following discussion addresses further errors in the Section 103 rejections.

2. The Section 103(a) rejection of claims 4 and 5 over the '894 reference in view of the '450 reference must also be reversed for reasons stated above in connection with the rejection of claim 1 (upon which claims 4 and 5 depend), and further because the proposed combination does not provide correspondence to the claimed invention and is further unmotivated.

Appellant incorporates the above argument regarding the '894 reference's failure to provide correspondence to the limitations in claim 1, and accordingly submits that the Section 103 rejections of claims 4 and 5 are improper because they rely upon the same teachings in the '894 reference.

The Section 103 rejections must also be reversed because the '450 reference does not correspond to claim limitations directed to encapsulation portions that extend between a spacer and a portion of second semiconductor material, above which said encapsulation portions is deposited. Specifically, the cited material 420 does not correspond to the claimed encapsulation portions. As is clearly shown in Figure 4 of the '450 reference, the material 420 does not extend between semiconductor material 314 and sidewall spacer 318 and thus fails to correspond to the claims as asserted. The Examiner again appears to be attempting to show correspondence to portions 8 and 9 of FIG. 7 in the instant application (copied above), but fails to show correspondence to the claimed second material and its arrangement (*e.g.*, as relative to 6 and 7 in FIG. 7). Therefore, the Section 103(a) rejections of claims 4 and 5 are improper and must be reversed.

3. The Section 103(a) rejection of claims 7-11 over the '450 reference in view of the '100 and '894 references must also be reversed because the rejection relies upon asserted teachings of the combination of the '450 and '894 references that do not correspond to the claimed invention as discussed above, and further because the combination of all three references is unmotivated.

Appellant incorporates the above arguments regarding the '894 reference's failure to provide correspondence to the limitations in claim 1, and regarding the combination of the '894 and '450 reference's failure to provide correspondence to limitations in claims 4 and 5, as applicable to the rejections of claims 7-11. The Section 103 rejection of claims 7-11 is also improper for reasons discussed above as based upon the Examiner's erroneous assertion that items 8 and 9 of Fig. 7 correspond to the claimed second semiconductor material, also as discussed above in relation to the § 102(b) rejection of claim 1. Appellant accordingly submits that the Section 103 rejections of claims 7-11 are improper because they rely upon the same alleged teachings and erroneous rejections made in connection with the Section 102 rejection over the '894 reference and/or the Section 103 rejection over the combination of the '894 and '450 references.

The Section 103(a) rejection of claims 7-10 must also be reversed because the cited portions of the '450 and '100 references do not teach or suggest various aspects of the claimed invention as asserted. Regarding the '450 reference, the cited portions therein do not teach or suggest claim limitations directed to removing two lateral parts of a first semiconductor material, where each lateral part extends between a substrate and a spacer up to the opposite sides of a gate electrode. As is clearly shown by the '450 reference in Figure 3B and relevant to the cited portions therein, recesses 312 in substrate 300 do not extend between the substrate 300 and spacers 310, and further do not extend up to the sidewalls of gate electrode 306.

Regarding the '100 reference, the cited portions therein do not teach or suggest claim limitations directed to forming a portion of a second semiconductor material that extends up to opposite sides of a gate electrode. For instance, referring to Figure 3B, cited material 318 does not extend up to the sidewalls of gate electrode 306. Rather, the material 318 extends up to spacer 314, which is formed along the sidewalls of a gate electrode 306, and further appears to be defined by the spacer (*i.e.*, as manufactured in

subsequent steps represented in Figures 3d, 3e and 3f). The cited portions of the '100 reference thus cannot correspond to the claimed invention as asserted in the Office Action.

Appellant further submits that the § 103(a) rejection of claims 7-10 is erroneous because none of the cited references teaches or suggests heating the portions of second semiconductor material to a temperature that is between the melting points of the first and second semiconductor materials, and so that portions of the second material contain electrical carriers with concentrations lower than that of deeper source and drain regions. The cited portions of the '894 reference asserted as teaching the claimed heating simply discuss an anneal but fail to discuss any claimed melting-point based heating as claimed (*see, e.g.,* column 13:20-45). The Examiner's response to arguments in the Final Office Action appear to (again) improperly rely upon allegedly inherent functions, in asserting that the '894 reference "implicitly anticipates the limitations of claims 7-10" but fails to show (or even mention) heating to a temperature that is between the aforesaid melting points, or that such limitations would necessarily flow from the teachings. These assertions therefore fail to provide correspondence to all claim limitations, and are in violation of the M.P.E.P. and relevant law relative to such assertions of inherency as discussed above.

In addition to the above, heating the device as cited in the '894 reference cannot result in the claimed second portion having a lower carrier concentration, as the portions of the '100 reference cited as corresponding to the claimed electrical carrier concentrations, because such an anneal would rely upon carriers in the cited upper portions therein. For example, Figure 3h and the corresponding discussion indicate that carriers diffuse from the region 318 into the area 312 to extend the deeper region 310, where such diffusion occurs from areas of higher concentration to areas of lower concentration. As such, the carrier concentration of cited region 310 is not higher than the carrier concentration of region 318.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-11 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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Respectfully Submitted,

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/554,067)

1. A semiconductor device comprising:

a gate electrode and a gate insulating layer produced on a part of the surface of a substrate of a first semiconductor material having a given melting point, and surrounded by an insulating spacer in a plane parallel to the surface of the substrate, the gate insulating layer being disposed between the substrate and the gate electrode, and

a source region and a drain region situated under the surface of the substrate at the level of two opposite sides of the gate electrode, respectively, each region containing electrical carriers of the same given type, with respective first concentrations, and each region comprising a portion of a second semiconductor material disposed on the substrate below the level of the gate insulating layer in a direction perpendicular to the surface of the substrate, each portion of second material extending at least partially between the substrate and the spacer, substantially as far as a limit coming in line, in said perpendicular direction, with one side of the gate electrode, said portions of second material being doped with doping elements in order to create electrical carriers of said given type with second concentrations less than said first concentrations, and said portions of second material having a melting point lower than the melting point of the first material.

2. A device as claimed in claim 1, in which said portions of second material have an ability to absorb a light radiation greater than the absorption ability of the first material for the same light radiation.

3. A device as claimed in claim 1, in which the first material is based on silicon and the second material is based on germanium or based on an alloy of silicon and germanium.

4. A device as claimed in claim 1, also comprising two encapsulation portions of said second material, disposed respectively over the portions of second material, on a side opposite to the substrate.

5. A device as claimed in claim 4, in which each encapsulation portion extends between the spacer and the portion of second material above which said encapsulation portion is disposed, substantially as far as a limit situated in line, in said direction perpendicular to the surface of the substrate, with the side of the gate electrode corresponding to said second encapsulation portion.

6. A device as claimed in claim 1, characterized in that said device is an MOS transistor.

7. A method of manufacturing a semiconductor device, comprising the following steps:

a) a gate insulating layer is formed on a part of a surface of a substrate of a first semiconductor material having a given melting point;

b) a gate electrode is formed on top of the gate insulating layer;

c) an insulating spacer is formed, disposed around the gate insulating layer and the gate electrode, parallel to the surface of the substrate;

d) two surface films of the first material are removed respectively in two lateral parts of the surface of the substrate situated on two opposite sides of the surface part of the substrate carrying the gate insulating layer and the gate electrode, each lateral part extending between the substrate and the spacer substantially as far as a limit coming in line with one of the opposite sides of the gate electrode, in a direction perpendicular to the surface of the substrate;

e) a source region and a drain region are formed, each region being situated below the surface of the substrate at a level of said two lateral parts of the surface of the substrate, respectively, each region containing electrical carriers of the same given type with respective first concentrations;

f) there is formed on the substrate, in each lateral part, a portion of a second semiconductor material substantially as far as a limit coming in line, in said perpendicular direction, with the opposite side of the gate electrode corresponding to said lateral part, said portions of second material containing doping elements in order to create electrical

carriers of the given type, and having a melting point lower than the melting point of the first material;

g) the portions of second material are heated to a temperature intermediate between the respective melting points of the first and second materials, so that the portions of second material contain electrical carriers with second concentrations lower than said first concentrations.

8. A method as claimed in claim 7, according to which, during step g), said portions of second material are heated using a laser beam.

9. A method as claimed in claim 7, according to which, after step f), encapsulation portions are deposited respectively on top of said portions of second material, on a side opposite to the substrate.

10. A method as claimed in claim 7, according to which step e) is performed before step d).

11. A method as claimed in claim 7, wherein steps a) through g) are performed successively.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.